```
RCS file: /s6/cvsroot/euterpe/.checkoutrc,v
Working file: .checkoutrc
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
.checkoutrc
----------------------------
revision 1.2
date: 1995/07/08 20:08:14;  author: chip;  state: Exp;  lines: +1 -6
remove obsolete comment. tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 23
description:
top level BOM
----------------------------
revision 3.921
date: 1995/07/13 23:23:52;  author: vanthof;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      lid_euterpe_1.ly
      vlsi.cko
      vlsi.log

releasing lid_euterpe_1.ly vlsi.cko vlsi.log
----------------------------
revision 3.920
date: 1995/07/13 07:05:03;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
```

```
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 3.919
date: 1995/07/12 20:37:16;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools

cmpregcommit: support for magic commit to terminate register comparison
processing
----------------------------
revision 3.918
date: 1995/07/12 19:05:58;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      Makefile

Added analyze of i_s in compv
----------------------------
revision 3.917
date: 1995/07/12 18:57:04;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

do magic commit to r6 of 0xcafe to tell cmpregcommit we are done
----------------------------
revision 3.916
date: 1995/07/12 18:54:04;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      c_euterpe_wrap.parm

Added new parameter channel, changed address to be module
----------------------------
revision 3.915
date: 1995/07/11 21:24:26;  author: fwo;  state: Exp;  lines: +2 -2
Release Target: euterpe/baseplate

Add a cvs Id string to clockparms.m4.
----------------------------
revision 3.914
date: 1995/07/09 17:04:14;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hcpll

Replace .'s with _'s in test names
----------------------------
revision 3.913
date: 1995/07/09 00:13:19;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog

The id chip is being used by tbr.
pick up some -base files for top level route
----------------------------
revision 3.912
date: 1995/07/08 23:20:41;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog
      Makefile

The id chip is being used by tbr.
previous release had syntax error
----------------------------
```

```
revision 3.911
date: 1995/07/08 19:41:55;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

The id chip is being used by tbr.
just cleaning up a bunch of .checkoutrc files
----------------------------
revision 3.910
date: 1995/07/08 19:26:49;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.909
date: 1995/07/08 19:24:12;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.908
date: 1995/07/08 19:21:20;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.907
date: 1995/07/08 19:19:15;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.906
date: 1995/07/08 19:17:07;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.905
date: 1995/07/08 19:15:03;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.904
date: 1995/07/08 19:05:03;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.903
```

```
date: 1995/07/08 19:02:39;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.902
date: 1995/07/08 18:59:49;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.901
date: 1995/07/08 18:56:06;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.900
date: 1995/07/08 18:50:12;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.899
date: 1995/07/08 18:41:56;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog
      Makefile

The id chip is being used by tbr.
Remove explicit display setting
=============================================================================

RCS file: /s6/cvsroot/euterpe/baseplate/BOM,v
Working file: baseplate/BOM
head: 33.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 65;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 25.0
date: 1995/07/11 21:24:09;  author: fwo;  state: Exp;  lines: +1 -1
Release Target: euterpe/baseplate

Add a cvs Id string to clockparms.m4.
----------------------------
revision 24.1
date: 1995/07/11 21:24:02;  author: fwo;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/baseplate/clockparms.m4,v
Working file: baseplate/clockparms.m4
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/07/11 21:14:32;  author: fwo;  state: Exp;  lines: +1 -0
Add an Id string so we can tell the version of this file.
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/BOM,v
Working file: compass/BOM
head: 7.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 67;    selected revisions: 1
description:
----------------------------
revision 4.3
date: 1995/07/13 23:23:37;  author: vanthof;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      lid_euterpe_1.ly
      vlsi.cko
      vlsi.log

releasing lid_euterpe_1.ly vlsi.cko vlsi.log
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/BOM,v
Working file: compass/layouts/BOM
head: 27.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79;    selected revisions: 1
description:
releasebom adding BOM
----------------------------
revision 18.3
date: 1995/07/13 23:23:28;  author: vanthof;  state: Exp;  lines: +4 -4
Release Target: euterpe/compass/layouts
      lid_euterpe_1.ly
      vlsi.cko
      vlsi.log

releasing lid_euterpe_1.ly vlsi.cko vlsi.log
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 3
description:
----------------------------
revision 4.197
date: 1995/07/12 20:36:52;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools

cmpregcommit: support for magic commit to terminate register comparison
processing
----------------------------
revision 4.196
date: 1995/07/12 18:56:33;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

do magic commit to r6 of 0xcafe to tell cmpregcommit we are done
----------------------------
revision 4.195
date: 1995/07/09 17:03:56;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hcpll

Replace .'s with _'s in test names
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile,v
Working file: verify/Makefile
head: 3.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 2
description:
----------------------------
revision 3.18
date: 1995/07/13 22:28:54;  author: dit00;  state: Exp;  lines: +2 -1
Added make for tools/regdepend
----------------------------
revision 3.17
date: 1995/07/09 17:32:23;  author: lisar;  state: Exp;  lines: +2 -1
Added build of toplevel/hermes
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/status,v
Working file: verify/status
head: 3.64
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 64;    selected revisions: 4
```

```
description:
----------------------------
revision 3.29
date: 1995/07/13 20:07:54;  author: lisar;  state: Exp;  lines: +9 -0
Periodic checkin
----------------------------
revision 3.28
date: 1995/07/13 16:10:47;  author: dit00;  state: Exp;  lines: +49 -0
Periodic update
----------------------------
revision 3.27
date: 1995/07/10 16:29:21;  author: lisar;  state: Exp;  lines: +10 -0
Periodic checkin
----------------------------
revision 3.26
date: 1995/07/08 17:19:15;  author: lisar;  state: Exp;  lines: +1 -0
Periodic checkin
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 2
description:
----------------------------
revision 1.176
date: 1995/07/10 20:08:15;  author: dit00;  state: Exp;  lines: +2 -2
Add ltlbeasy.S, gtlbeasy.S
----------------------------
revision 1.175
date: 1995/07/09 17:30:30;  author: lisar;  state: Exp;  lines: +18 -20
Moved {g,l}tlbeasy, changed name of CONFIG list to VARIATIONS
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2075.S,v
Working file: verify/random/regdepend_r2075.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/13 17:00:03;  author: dit00;  state: Exp;
Add test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6552.S,v
Working file: verify/random/regdepend_r6552.S
head: 4.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/13 16:49:49;  author: dit00;  state: Exp;
Add test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7763.S,v
Working file: verify/random/regdepend_r7763.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/13 16:51:22;  author: dit00;  state: Exp;
Add test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7963.S,v
Working file: verify/random/regdepend_r7963.S
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/07/13 16:53:03;  author: dit00;  state: Exp;
Add test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/status,v
Working file: verify/random/status
head: 2.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 2.13
date: 1995/07/10 20:23:10;  author: dit00;  state: Exp;  lines: +28 -0
Periodic Update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/template,v
```

```
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 2
description:
----------------------------
revision 2.17
date: 1995/07/11 20:53:50;  author: dit00;  state: Exp;  lines: +2 -2
Periodic update
----------------------------
revision 2.16
date: 1995/07/08 22:25:16;  author: dit00;  state: Exp;  lines: +18 -18
Periodic update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/BOM,v
Working file: verify/standalone/BOM
head: 6.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 1
description:
----------------------------
revision 4.35
date: 1995/07/09 17:03:46;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/hcpll

Replace .'s with _'s in test names
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/BOM,v
Working file: verify/standalone/hcpll/BOM
head: 5.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 5.0
date: 1995/07/09 17:03:36;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/standalone/hcpll

Replace .'s with _'s in test names
----------------------------
revision 4.1
date: 1995/07/09 17:03:29;  author: lisar;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/Makefile,v
Working file: verify/standalone/hcpll/Makefile
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/07/09 17:02:34;  author: lisar;  state: Exp;  lines: +21 -10
Take out .'s and use _'s. IKOS tools don't like
multiple .'s.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/clean-request,v
Working file: verify/standalone/hcpll/clean-request
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/07/09 17:02:36;  author: lisar;  state: Exp;  lines: +3 -0
Take out .'s and use _'s. IKOS tools don't like
multiple .'s.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hcpll/hcpll.pl,v
Working file: verify/standalone/hcpll/hcpll.pl
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/07/09 17:02:37;  author: lisar;  state: Exp;  lines: +5 -3
Take out .'s and use _'s. IKOS tools don't like
multiple .'s.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/BOM,v
Working file: verify/tools/BOM
head: 13.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 90;    selected revisions: 3
description:
```

```
releasebom adding BOM
----------------------------
revision 10.0
date: 1995/07/12 20:36:35;  author: doi;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/tools

cmpregcommit: support for magic commit to terminate register comparison
processing
----------------------------
revision 9.2
date: 1995/07/12 20:36:27;  author: doi;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 9.1
date: 1995/07/12 18:56:17;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/tools/regdepend

do magic commit to r6 of 0xcafe to tell cmpregcommit we are done
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/cmpregcommit,v
Working file: verify/tools/cmpregcommit
head: 3.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 3.7
date: 1995/07/12 20:35:06;  author: doi;  state: Exp;  lines: +21 -1
add support for magic commit of 0xcafe to register 6 to terminate the comparison
when the -M option is used
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/stgen,v
Working file: verify/tools/stgen
head: 5.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 5.10
date: 1995/07/12 18:55:08;  author: doi;  state: Exp;  lines: +2 -1
do magic commit to r6 of 0xcafe to tell cmpregcommit we are done
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/regdepend/BOM,v
Working file: verify/tools/regdepend/BOM
head: 26.0
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 50;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 25.0
date: 1995/07/12 18:56:00;  author: doi;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/tools/regdepend

do magic commit to r6 of 0xcafe to tell cmpregcommit we are done
----------------------------
revision 24.1
date: 1995/07/12 18:55:49;  author: doi;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/regdepend/regdepend.c,v
Working file: verify/tools/regdepend/regdepend.c
head: 1.29
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 29;    selected revisions: 1
description:
----------------------------
revision 1.28
date: 1995/07/12 18:53:00;  author: doi;  state: Exp;  lines: +7 -2
do magic commit to r6 of 0xcafe to tell cmpregcommit we are done
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 2
description:
----------------------------
revision 1.176
date: 1995/07/10 20:08:15;  author: dit00;  state: Exp;  lines: +2 -2
Add ltlbeasy.S, gtlbeasy.S
----------------------------
revision 1.175
date: 1995/07/09 17:30:30;  author: lisar;  state: Exp;  lines: +18 -20
Moved {g,l}tlbeasy, changed name of CONFIG list to VARIATIONS
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cp_debug.sig,v
Working file: verify/toplevel/cp_debug.sig
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 41.2
date: 1995/07/13 00:32:30;  author: jeffm;  state: Exp;  lines: +9 -1
Add signals.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermes_Ibash.S,v
Working file: verify/toplevel/hermes_Ibash.S
head: 35.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 35.4
date: 1995/07/09 17:00:56;  author: lisar;  state: Exp;  lines: +18 -27
Fixed an alignment error in thread 4
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/icachemiss.S,v
Working file: verify/toplevel/icachemiss.S
head: 27.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 27.7
date: 1995/07/12 19:08:05;  author: jeffm;  state: Exp;  lines: +2 -2
Uninitialized tag.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 5
description:
----------------------------
revision 1.123
date: 1995/07/13 22:38:57;  author: dit00;  state: Exp;  lines: +41 -41
Fixed some more time elements to be more friendly to Ikos
----------------------------
revision 1.122
date: 1995/07/13 06:26:18;  author: lisar;  state: Exp;  lines: +7 -6
Added vmunix
----------------------------
revision 1.121
```

```
date: 1995/07/12 21:12:56;  author: dit00;  state: Exp;  lines: +43 -43
Periodic update
----------------------------
revision 1.120
date: 1995/07/10 16:24:54;  author: lisar;  state: Exp;  lines: +5 -2
try>run
----------------------------
revision 1.119
date: 1995/07/09 17:30:36;  author: lisar;  state: Exp;  lines: +12 -13
Moved {g,l}tlbeasy, changed name of CONFIG list to VARIATIONS
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 19
description:
top level verilog BOM
----------------------------
revision 4.3
date: 1995/07/13 07:04:41;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 4.2
date: 1995/07/12 19:05:31;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      Makefile

Added analyze of i_s in compv
----------------------------
revision 4.1
date: 1995/07/12 18:53:31;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      c_euterpe_wrap.parm
```

```
Added new parameter channel, changed address to be module
----------------------------
revision 4.0
date: 1995/07/09 00:12:45;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog

The id chip is being used by tbr.
pick up some -base files for top level route
----------------------------
revision 3.678
date: 1995/07/09 00:12:27;  author: chip;  state: Exp;  lines: +3 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 3.677
date: 1995/07/08 23:20:13;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog
      Makefile

The id chip is being used by tbr.
previous release had syntax error
----------------------------
revision 3.676
date: 1995/07/08 19:41:17;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

The id chip is being used by tbr.
just cleaning up a bunch of .checkoutrc files
----------------------------
revision 3.675
date: 1995/07/08 19:26:16;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.674
date: 1995/07/08 19:23:52;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.673
date: 1995/07/08 19:21:02;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.672
date: 1995/07/08 19:18:56;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
```

```
revision 3.671
date: 1995/07/08 19:16:45;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.670
date: 1995/07/08 19:14:42;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 3.669
date: 1995/07/08 19:04:43;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.668
date: 1995/07/08 19:02:17;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.667
date: 1995/07/08 18:59:28;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.666
date: 1995/07/08 18:55:49;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ctiod

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.665
date: 1995/07/08 18:49:56;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 3.664
date: 1995/07/08 18:41:37;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog
      Makefile

The id chip is being used by tbr.
Remove explicit display setting
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/Makefile,v
Working file: verilog/Makefile
head: 1.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 5
description:
Makefile
----------------------------
revision 1.7
date: 1995/07/09 03:05:24;  author: chip;  state: Exp;  lines: +2 -2
get rid of -j.  problem in the cg section.  tbr
----------------------------
revision 1.6
date: 1995/07/08 23:19:12;  author: chip;  state: Exp;  lines: +3 -3
oops, wrong shell syntax
----------------------------
revision 1.5
date: 1995/07/08 23:14:11;  author: chip;  state: Exp;  lines: +2 -2
correct typo in last checkin
----------------------------
revision 1.4
date: 1995/07/08 20:05:46;  author: chip;  state: Exp;  lines: +3 -2
make updatedirs before gards. tbr.
----------------------------
revision 1.3
date: 1995/07/08 18:40:18;  author: chip;  state: Exp;  lines: +2 -2
remove explicit display setting.  tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 19
description:
----------------------------
revision 333.0
date: 1995/07/13 07:04:14;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
```

```
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 332.3
date: 1995/07/13 07:03:57;  author: tbr;  state: Exp;  lines: +13 -13
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 332.2
date: 1995/07/12 19:05:09;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      Makefile

Added analyze of i_s in compv
----------------------------
revision 332.1
date: 1995/07/12 18:53:04;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      c_euterpe_wrap.parm

Added new parameter channel, changed address to be module
----------------------------
revision 332.0
date: 1995/07/09 00:10:57;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog

The id chip is being used by tbr.
pick up some -base files for top level route
----------------------------
revision 331.1
date: 1995/07/09 00:10:37;  author: chip;  state: Exp;  lines: +7 -7
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 331.0
date: 1995/07/08 19:40:53;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

The id chip is being used by tbr.
just cleaning up a bunch of .checkoutrc files
----------------------------
revision 330.13
date: 1995/07/08 19:40:38;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 330.12
date: 1995/07/08 19:25:48;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 330.11
```

```
date: 1995/07/08 19:23:33;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 330.10
date: 1995/07/08 19:20:45;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 330.9
date: 1995/07/08 19:18:39;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 330.8
date: 1995/07/08 19:16:25;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 330.7
date: 1995/07/08 19:14:24;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 330.6
date: 1995/07/08 19:04:25;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 330.5
date: 1995/07/08 19:01:55;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 330.4
date: 1995/07/08 18:59:05;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 330.3
date: 1995/07/08 18:55:31;  author: chip;  state: Exp;  lines: +2 -2
```

```
Release Target: euterpe/verilog/bsrc/ctiod

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 330.2
date: 1995/07/08 18:49:41;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 1
description:
----------------------------
revision 1.250
date: 1995/07/12 19:04:45;  author: lisar;  state: Exp;  lines: +2 -1
Added analyze of i_s in compv
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 1
description:
----------------------------
revision 40.95
date: 1995/07/13 05:23:05;  author: tbr;  state: Exp;  lines: +20 -7
added kludge final-report target for use after manual route clean up
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/analog_euterpe.hwc,v
Working file: verilog/bsrc/analog_euterpe.hwc
head: 35.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 35.6
date: 1995/07/09 17:16:10;  author: chip;  state: Exp;  lines: +4 -4
reduce with of vddep0/1 to 10.5 to be compatible with new pads, per geert.  tbr
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/c_euterpe_wrap.parm,v
Working file: verilog/bsrc/c_euterpe_wrap.parm
head: 183.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 183.8
date: 1995/07/12 18:52:27;  author: lisar;  state: Exp;  lines: +18 -8
Added new parameter channel, changed address to be module
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 312.11
date: 1995/07/13 05:29:06;  author: tbr;  state: Exp;  lines: +36388 -35316
patched for changes in rg and io
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
----------------------------
revision 312.12
date: 1995/07/13 05:34:34;  author: tbr;  state: Exp;  lines: +734 -700
patched for changes in rg and io
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 312.11
```

```
date: 1995/07/13 05:36:39;  author: tbr;  state: Exp;  lines: +3921 -3905
patched for changes in rg and io
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;   selected revisions: 1
description:
----------------------------
revision 6.428
date: 1995/07/10 23:54:48;  author: dickson;  state: Exp;  lines: +9 -5
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe_wrap.V,v
Working file: verilog/bsrc/euterpe_wrap.V
head: 15.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 1
description:
----------------------------
revision 15.97
date: 1995/07/11 04:17:11;  author: lisar;  state: Exp;  lines: +14 -1
Add inverters for channel 1
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_h_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_h_euterpe_wrap.tb
head: 325.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 325.3
date: 1995/07/11 04:17:54;  author: lisar;  state: Exp;  lines: +3 -3
Config file name is .in
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;   selected revisions: 1
```

```
description:
releasebom adding BOM
----------------------------
revision 92.0
date: 1995/07/08 19:32:55;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

The id chip is being used by tbr.
just cleaning up a bunch of .checkoutrc files
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 83.0
date: 1995/07/13 06:54:11;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 82.1
date: 1995/07/13 06:54:01;  author: tbr;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerberus.V,v
Working file: verilog/bsrc/ce/cerberus.V
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 63;    selected revisions: 1
description:
----------------------------
revision 1.56
date: 1995/07/10 23:53:37;  author: dickson;  state: Exp;  lines: +6 -5
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/cerbtest.V,v
Working file: verilog/bsrc/ce/cerbtest.V
head: 1.46
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 1.43
date: 1995/07/10 23:53:40;  author: dickson;  state: Exp;  lines: +8 -6
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ceregcore.V,v
Working file: verilog/bsrc/ce/ceregcore.V
head: 1.44
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 44;    selected revisions: 1
description:
----------------------------
revision 1.42
date: 1995/07/10 23:53:43;  author: dickson;  state: Exp;  lines: +36 -35
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/.checkoutrc,v
Working file: verilog/bsrc/ctiod/.checkoutrc
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/07/08 18:52:10;  author: chip;  state: Exp;  lines: +2 -2
remove explicit display setting. tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ctiod/BOM,v
Working file: verilog/bsrc/ctiod/BOM
head: 31.0
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 61;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 31.0
date: 1995/07/08 18:55:14;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/ctiod

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 30.1
date: 1995/07/08 18:55:07;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/.checkoutrc,v
Working file: verilog/bsrc/dr/.checkoutrc
head: 32.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 2
description:
----------------------------
revision 32.6
date: 1995/07/08 19:12:43;  author: chip;  state: Exp;  lines: +2 -2
reverse order of redirections
----------------------------
revision 32.5
date: 1995/07/08 18:57:13;  author: chip;  state: Exp;  lines: +2 -2
remove explicit DISPLAY setting . tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/dr/BOM,v
Working file: verilog/bsrc/dr/BOM
head: 77.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 155;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 75.0
date: 1995/07/08 19:14:06;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 74.1
```

```
date: 1995/07/08 19:13:59;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 74.0
date: 1995/07/08 18:58:42;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/dr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 73.1
date: 1995/07/08 18:58:34;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/.checkoutrc,v
Working file: verilog/bsrc/es/.checkoutrc
head: 45.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 45.3
date: 1995/07/08 19:15:38;  author: chip;  state: Exp;  lines: +2 -2
reverse order of redirections
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;   selected revisions: 2
description:
----------------------------
revision 97.0
date: 1995/07/08 19:16:06;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 96.1
date: 1995/07/08 19:15:58;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/.checkoutrc,v
Working file: verilog/bsrc/gt/.checkoutrc
head: 39.5
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 39.5
date: 1995/07/08 19:01:06;  author: chip;  state: Exp;  lines: +2 -2
remove explicit DISPLAY setting . tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 194;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 98.0
date: 1995/07/08 19:01:35;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 97.1
date: 1995/07/08 19:01:26;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/.checkoutrc,v
Working file: verilog/bsrc/hc/.checkoutrc
head: 35.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 35.10
date: 1995/07/08 19:03:33;  author: chip;  state: Exp;  lines: +3 -3
remove explicit DISPLAY setting . tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 4
description:
```

```
releasebom adding BOM
----------------------------
revision 123.0
date: 1995/07/13 06:57:56;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 122.1
date: 1995/07/13 06:57:46;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 122.0
date: 1995/07/08 19:04:06;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 121.1
date: 1995/07/08 19:03:58;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/Makefile,v
Working file: verilog/bsrc/hc/Makefile
head: 1.30
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 30;    selected revisions: 1
description:
----------------------------
revision 1.30
date: 1995/07/10 01:35:19;  author: tbr;  state: Exp;  lines: +1 -6
get rid of explicit display setting, and doi_verilog nit
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_device.V,v
```

```
Working file: verilog/bsrc/hc/hc_device.V
head: 8.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 8.10
date: 1995/07/12 17:12:17;  author: doi;  state: Exp;  lines: +4 -3
The hermes model now requires an additional parameter be
passed to the h_init routine.  This parameter will
tell the hermes model what channel it is attached to.
This parameter is used *only* when the hermes model
is reading it's configuration file (if any) to determine if
a particular option is targeted at this device.

THIS PARAMETER DOES NOT DIRECTLY ALTER THE OPERATION OF THE HERMES
MODEL IN ANY WAY.

Also, this file is being copied and checked into the chaos
tree.  It should be removed from the euterpe tree once
the sources that use this file uses the chaos version.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/.checkoutrc,v
Working file: verilog/bsrc/icc/.checkoutrc
head: 15.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 15.4
date: 1995/07/08 19:17:55;  author: chip;  state: Exp;  lines: +2 -2
reverse order of redirections
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 49.0
date: 1995/07/08 19:18:21;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/icc

The id chip is being used by tbr.
```

```
reverse order of redirections in .checkoutrc
----------------------------
revision 48.1
date: 1995/07/08 19:18:13;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/BOM,v
Working file: verilog/bsrc/io/BOM
head: 48.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 94;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 46.0
date: 1995/07/13 06:59:02;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 45.1
date: 1995/07/13 06:58:52;  author: tbr;  state: Exp;  lines: +7 -7
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/Makefile,v
Working file: verilog/bsrc/io/Makefile
head: 1.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 1.18
```

```
date: 1995/07/10 23:54:14;  author: dickson;  state: Exp;  lines: +6 -1
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io0_control.pim,v
Working file: verilog/bsrc/io/io0_control.pim
head: 22.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 22.10
date: 1995/07/10 23:54:16;  author: dickson;  state: Exp;  lines: +2 -0
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io1_control.pim,v
Working file: verilog/bsrc/io/io1_control.pim
head: 22.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 22.6
date: 1995/07/10 23:54:18;  author: dickson;  state: Exp;  lines: +3 -1
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io_buf_8.V,v
Working file: verilog/bsrc/io/io_buf_8.V
head: 31.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 31.2
date: 1995/07/10 23:54:20;  author: dickson;  state: Exp;  lines: +4 -2
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/io_ififo.V,v
Working file: verilog/bsrc/io/io_ififo.V
head: 6.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
```

```
description:
----------------------------
revision 6.4
date: 1995/07/10 23:54:22;  author: dickson;  state: Exp;  lines: +6 -4
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/iorate.V,v
Working file: verilog/bsrc/io/iorate.V
head: 3.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 3.12
date: 1995/07/10 23:54:23;  author: dickson;  state: Exp;  lines: +4 -3
single end rawdata from hc0/hc1 to cerberus
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/.checkoutrc,v
Working file: verilog/bsrc/lt/.checkoutrc
head: 56.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 56.3
date: 1995/07/08 19:20:05;  author: chip;  state: Exp;  lines: +2 -2
reverse order of redirections
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 98.0
date: 1995/07/08 19:20:27;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/lt

The id chip is being used by tbr.
reverse order of redirections in .checkoutrc
----------------------------
revision 97.1
date: 1995/07/08 19:20:20;  author: chip;  state: Exp;  lines: +2 -2
```

```
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/.checkoutrc,v
Working file: verilog/bsrc/nb/.checkoutrc
head: 46.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 46.7
date: 1995/07/08 19:22:09;  author: chip;  state: Exp;  lines: +2 -2
remove explicit display setting. tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v
Working file: verilog/bsrc/nb/BOM
head: 130.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 261;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 129.0
date: 1995/07/08 19:23:11;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/nb

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 128.1
date: 1995/07/08 19:23:02;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 2
description:
----------------------------
revision 135.0
date: 1995/07/13 07:01:29;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


analog_euterpe.hwc: change to 10.5 wires
```

```
euterpe.V: single end rawdata
*base*: updated for rg and io changes below

rg/rg.pim: put back alignment marks

hc/hc_device.V: add new parameter

ce/cerberus.V
ce/cerbtest.V
ce/ceregcore.V: single end rawdata

io/Makefile
io0_control.pim
io1_control.pim
io_buf_8.V
iorate.V:   single end rawdata
----------------------------
revision 134.1
date: 1995/07/13 07:01:18;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 2
description:
----------------------------
revision 82.31
date: 1995/07/13 20:26:25;  author: dickson;  state: Exp;  lines: +17 -17
avoid toplevel collisions with gf block
----------------------------
revision 82.30
date: 1995/07/11 03:23:10;  author: dickson;  state: Exp;  lines: +384 -384
aligned all mux5 groups to open up more verticle routing tracks.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/.checkoutrc,v
Working file: verilog/bsrc/sr/.checkoutrc
head: 24.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 24.7
date: 1995/07/08 19:24:45;  author: chip;  state: Exp;  lines: +2 -2
remove explicit display setting. tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v
```

```
Working file: verilog/bsrc/sr/BOM
head: 75.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 74.0
date: 1995/07/08 19:25:21;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/sr

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 73.1
date: 1995/07/08 19:25:11;  author: chip;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/.checkoutrc,v
Working file: verilog/bsrc/uu/.checkoutrc
head: 79.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 79.4
date: 1995/07/08 18:48:05;  author: chip;  state: Exp;  lines: +2 -2
remove explicit display setting. tbr
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 2
description:
----------------------------
revision 214.0
date: 1995/07/08 18:49:24;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

The id chip is being used by tbr.
remove explicit display setting from .checkoutrc
----------------------------
revision 213.1
date: 1995/07/08 18:48:37;  author: chip;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
```

```
      .checkoutrc

The id chip is being used by tbr.
remove
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/lvs/BOM,v
Working file: verilog/lvs/BOM
head: 3.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 2
description:
----------------------------
revision 2.0
date: 1995/07/09 00:11:53;  author: chip;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog

The id chip is being used by tbr.
pick up some -base files for top level route
----------------------------
revision 1.2
date: 1995/07/09 00:11:41;  author: chip;  state: Exp;  lines: +2 -1
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```